CODE: 17CD04103

M. Tech I Year I Semester Supplementary Examinations, May 2018

CMOS DIGITAL IC DESIGN
(VLSISD)

Time : 3 hours Max Marks : 60

Answer all **five** units. (5 x 12 = 60 Marks)

UNIT-I

1. (a) Draw the CMOS Inverter; Explain the operation with transfer characteristics.

(b) Explain the concept of ratioed logic and pass transistor with suitable example.

OR

2. (a) Draw the Pseudo NMOS 2-input NOR gate and explain the operation with functional table.

(b) Explain the dynamic behavior of CMOS inverter by computing the capacitances and propagation delays.

UNIT-II

3. (a) Design and explain the operation of 2 input NMOS NOR gate.

(b) Realize the following Boolean expression using NMOS and CMOS logic.
Y'=A(B+C)+DE

OR

4. (a) Realize 2 to 1 line multiplexer using CMOS transmission gate.

(b) Explain with neat circuit diagram CMOS implementation of carry look ahead adder in dynamic logic.

UNIT-III

5. (a) Draw the circuit diagram of edge triggered DFF and explain operation with timing diagram.

(b) Draw and explain the operation of clocked CMOS SR Latch using NOR gate version.

OR

6. (a) Draw the D Latch using CMOS logic and explain the operation.

(b) Draw and explain the operation of CMOS SR Latch.

UNIT-IV

7. (a) Illustrate the cascading problem in dynamic CMOS logic.

(b) Explain the concept of charge storage and charge leakage with respect to pass transistor logic.

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OR

8. (a) Compare conventional CMOS logic with domino CMOS logic. Illustrate with example.

(b) Draw the 3-input NAND gate dynamic CMOS Logic circuit and explain the operation.

UNIT-V

9. (a) Illustrate random access memory array organization with neat block diagram.

(b) Explain the leakage currents in DRAM cells and refresh operation.

OR

10. (a) Describe the leakage current in SRAM.

(b) Explain NAND FLASH Memory.

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