

**CODE: 17CD04102**

M. Tech I Year I Semester Regular Examinations, February 2018

**CMOS ANALOG IC DESIGN**

**(VLSISD)**

Time: 3 hours

Max Marks: 60

Answer all **five** units. (5 x 12 = 60 Marks)

**UNIT-I**

1. (a) Explain the threshold voltage in MOS Transistor with equations..  
(b) Discuss the computer simulation models.

OR

2. (a) Describe the Large signal model for the MOS transistor.  
(b) Define and explain resistor IC Layout with neat sketches.

**UNIT-II**

3. (a) Draw the circuit diagram for voltage controlled MOS switch and explain its operation.  
(b) Describe the simple current mirror with degeneration helper using necessary equations.

OR

4. (a) Explain how voltage can be divided using active resistor.  
(b) Draw the circuit for standard cascade current sink and write its small signal model.

**UNIT-III**

5. (a) Develop and explain the small signal model for the active load inverter.  
(b) Illustrate voltage transfer function for the cascade amplifier.

OR

6. (a) Describe reduction of noise by offset cancellation technique..  
(b) With circuit explain differential current amplifier.

**UNIT-IV**

7. (a) Draw the schematic of folded cascode CMOS op-amp and illustrate the breaking of voltage to current, current to current and current to voltage stages.  
(b) Describe the compensation of op-amp that makes it completely independent of process and temperature variations.

OR

8. (a) Derive the expression for slew rate of CMOS op-amp.  
(b) Briefly explain the measurement techniques are used to measure CMRR, PSRR and slew rate of an op-amp.

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**UNIT-V**

9. (a) Explain the design aspect of two stage open loop comparator for slewing response.  
(b) With neat sketch explain the discrete time comparators.

OR

10. (a) Find the propagation delay time of an open loop comparator that has a dominant pole at  $10^3$  rad/sec, a dc gain of  $10^4$ , a slew rate of  $1\text{V}/\mu\text{sec}$ , and a binary output voltage swing of  $1\text{V}$ . Assume the applied input voltage is  $10\text{mV}$ .  
(b) Define and explain Autozeroing Technique to improve the performance of open loop comparator.

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