CODE: 17CD04103

M. Tech I Year I Semester Regular Examinations, February 2018

CMOS DIGITAL IC DESIGN

(VLSISD)

Time : 3 hours Max Marks : 60

Answer all **five** units. (5 x 12 = 60 Marks)

UNIT-I

1. (a) Design a Pseudo NMOS Inverter for 0.6 um technology.

(b) Explain about Typical Output high voltage and Typical Output low Voltage.

OR

2. Explain Briefly with suitable diagrams about Transistor Equivalency and verify when two transistors are parallel and series having equal lengths.

UNIT-II

3. Design and explain the operation of 2 Input NMOS NOR gate.

OR

4. Explain about Transmission gates with regions and design XOR circuit using Transmission gates.

UNIT-III

5. Explain the Behaviour of Bistable elements with neat diagrams.

OR

6. Explain About Clocked SR Latch and Clocked JK Latch.

UNIT-IV

7. Explain about Dynamic CMOS transmission gate logic with an example.

OR

8. Explain about Domino CMOS Logic with cascaded and explain an example.

UNIT-V

9. Explain Full CMOS SRAM cell and voltage levels for read and write operations.

OR

10. Explain about three transistors and one transistor DRAM with waveforms.

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