CODE: 17CD04104

M. Tech I Year I Semester Regular Examinations, February 2018

HARDWARE DESCRIPTION LANGUAGES
(VLSISD)

Time : 3 hours Max Marks : 60

Answer all **five** units. (5 x 12 = 60 Marks)

UNIT-I

1. (a) Explain with examples, the different data types supported by Verilog HDL.

(b) Explain the four levels of modeling supported by Verilog.

OR

2. (a) Explain the terms 'Inertial Delay' and 'Transport Delay' relevant to Verilog HDL models with suitable examples.

(b) Explain with examples the different Verilog Variables.

UNIT-II

3. (a) With an example, explain Behavioral Modeling of Verilog.

(b) Explain Blocking and Non-Blocking Assignments.

OR

4. (a) Explain how the Simulator Processes Blocking and Non-Blocking Procedural assignments.

(b) Explain the concepts of 'Constructs for activity flow control' Give the Behavioral description in Verilog HDL.

UNIT-III

5. (a) Implement the Behavioral model for Moore-type Finite State Machine using the Verilog HDL source code.

(b) With suitable example, explain the synthesis of Multi-cycle Operations.

OR

6. With suitable examples, explain the following.

i. Sequential Logic

ii. Combinational Logic

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UNIT-IV

7. (a) Draw the circuit diagram of switch level CMOS 2-input NAND gate and develop its source code.

(b) Explain in detail

i. NMOS switch

ii. PMOS switch

OR

8. (a) What are bidirectional Switches, explain the use of the following

i. Trans

ii. Trans if 0

iii. Trans if 1

(b) Explain the gate/switch declaration syntax

UNIT-V

9. (a) Give the behavioral description of MSI-based design hardware in VHDL. Draw the logic diagram.

(b) Differentiate between VHDL and Verilog with suitable examples.

OR

10. (a) Explain the top- down design approach in VHDL.

(b) Explain the following design procedures in VHDL.

a. Synthesis

b. Optimization

c. Place and Route

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