

CODE: 17CD04101

M. Tech I Year I Semester Regular Examinations, February 2018
STRUCTURAL DIGITAL SYSTEM DESIGN
(VLSISD)

Time: 3 hours

Max Marks: 60

Answer all **five** units. (5 x 12 = 60 Marks)

UNIT-I

1. (a) Illustrate the functionality of the following building blocks used for digital design with relevant figures and example
 - i. Full adder
 - ii. ALU
 - iii. Decoder
 - (b) Explain the features, functionality and implementation of JK flip flop. Show the two mixed-logic uses of the 74LS109 Dual JK Flip-Flop and describe various uses of JK Flip flop.
- OR
2. (a) Interpret the role and functionality of Comparator in the digital design. Illustrate how comparison of 8-bit quantities P and Q can be accomplished using the 74LS85 with relevant figure, notations and equation
 - (b) Explain the construction of a 12-bit binary counter using 74LS163 chips. For a 4-bit ripple counter, demonstrate how the output ripple can produce hazards in circuits that receive the outputs.

UNIT-II

3. (a) Explain top-down design methodology with example.
 - (b) Illustrate how refining of the Architecture and Control Algorithm is done with an example. Also discuss the challenges, benefits and effects of refining the architecture
- OR
4. (a) What is a state time? In a synchronous system, what determines the duration of the state time? Illustrate the purely sequential algorithm as an ASM chart of a sequence of states
 - (b) What is the difference between an ASM conditional branch and an ASM conditional output? Does one imply the other?

UNIT-III

5. (a) Illustrate the traditional Synthesis from an ASM Chart showing the figures of simple ASM with a state assignment and model of an encoded ASM state generator.
- (b) What are Asynchronous ASM? List the issues associated with asynchronous ASMs? Compare the advantages and drawbacks of synchronous and asynchronous ASMs.

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OR

6. (a) Illustrate the ROM-Based Method of ASM Synthesis with a neat figure of Implementation of the ASM using a ROM.
- (b) List and explain the features of various fault analysis tools

UNIT-IV

7. (a) Illustrate the ROM based micro-programmed implementation of the ASM with single qualifier per state using relevant example
- (b) Explain the features of the 2910 Micro program Sequencer with a neat figure of its internal architecture and twelve-bit data paths in the 2910 micro program sequencer

OR

8. (a) Explain the features and architecture of Logic Engine controller with a neat figure
- (b) Explain the design of micro programmed mini-computer showing the steps for developing a Micro program and the architecture of LD30

UNIT-V

9. Demonstrate the design of a single pulse showing the statement, algorithmic solution, combined architecture-algorithm solution, ASM and the implementation details

OR

10. Demonstrate the design of a serial bit clock showing the statement, algorithmic solution, combined architecture-algorithm solution, ASM and the implementation details
